TR-995

ELECTRONIC LONG-DELAY TIMER

Ira Marcus

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DIAMOND ORDNANCE FUZE LABORATORIES
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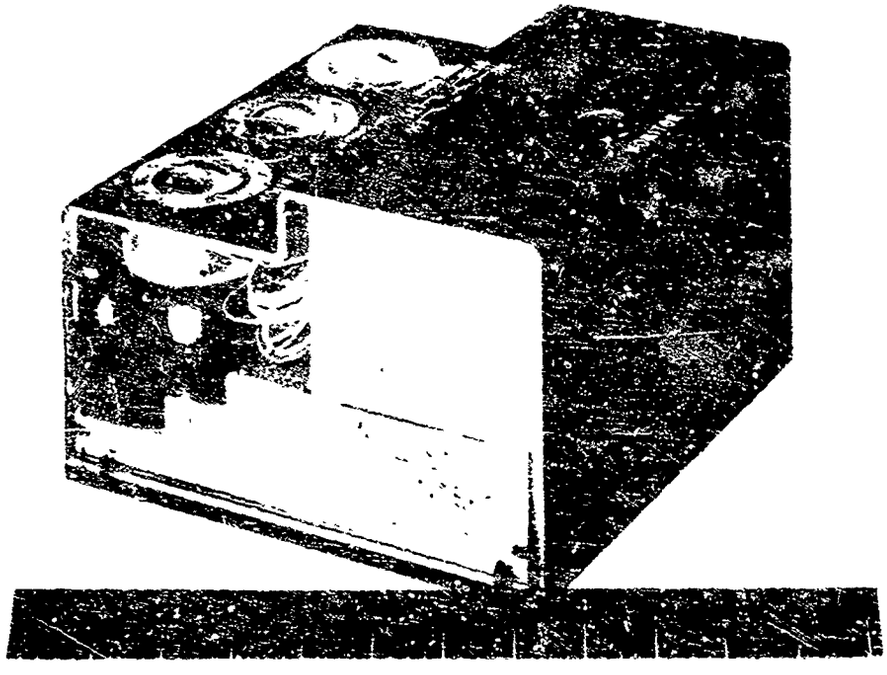
FOR THE COMMANDER:
Approved by

P. E. Landis
Chief, Laboratory 400



Frontispiece. 50-hour electronic timer 2038-61

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ABSTRACT

A settable all-electronic long-delay timer is described. The timer is settable in five-minute increments from five minutes to forty-nine hours fifty-five minutes. At the end of the set-in time a silicon controlled rectifier is latched on that is capable of delivering 2 amp at 6 v. The time remaining to fire may be read out upon command at any time. The time base is a 100.1 cps unijunction transistor oscillator. Countdown is by magnetic core shift registers. The total volume for the timer and its 100-hr power supply is 35 in^3.

1. INTRODUCTION

The electronic long-delay timer described herein was designed and built at DOFL to meet the following specifications:

(a) Provide an electrical output of 2 amp at 6 v at the end of a predetermined time.

(b) Be settable in 5-min increments from 5 min to 49 hr 55 min.

(c) Be capable of being reset.

(d) Have a provision for readout of any unexpired portion of the preset time.

(e) Contain its own power supply capable of 100-hr operation.

(f) Have a volume of 35 in^3. or less.

(g) Be capable of operation in any orientation.

(h) Operate over the temperature range -65°F to +160°F.

(i) Have a minimum timing accuracy of ±1 percent and a preferred timing accuracy of ±0.1 percent.

(j) Be incapable of being set below 5 min.

A block diagram of the system is shown in figure 1. The system consists of a 100.1-cps unijunction transistor oscillator followed by a core driver that drives four magnetic core shift registers in parallel. The four shift registers contain 11, 13, 14 and 15 stages.

The output of these shift registers feeds into a magnetic AND circuit. The AND circuit has an output once every 30,030 oscillator pulses and thus gives out an output pulse once every 5 min. A monitor circuit is included to indicate operation of the oscillator when the unit is timing. The input to the monitor is taken from the AND core following the 11- and 13-stage shift registers. The blinking

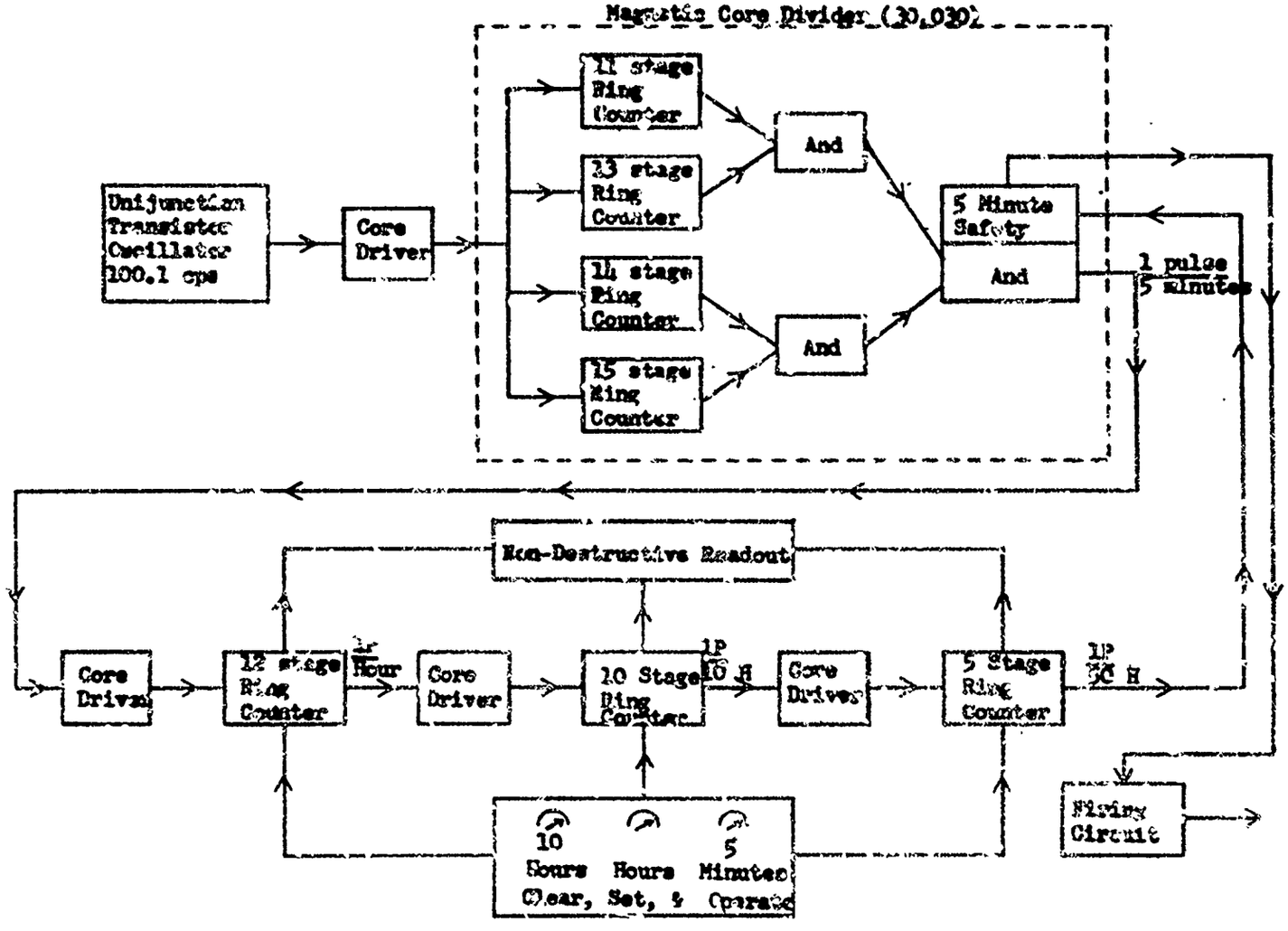


Figure 1. Block diagram of electronic long delay timer

rate of the monitor light is 1.43 sec per on-off cycle. The rate may be used as a rough check of the oscillator frequency (10 blinking cycles in 14.3 sec).

The output of the magnetic core AND circuit feeds three serial driver-shift-register combinations. The shift registers have 12, 10, and 5 stages. Each stage of the 12-stage register corresponds to 5 min and the output of the 12-stage ring is one pulse per hour. Similarly, each stage of the 10-stage ring corresponds to 1 hr and each stage of the 5-stage ring corresponds to 10 hr. When the firing time is initially set in, each ring has one bit inserted into the proper core. Readout of the time to go is accomplished by interrogation of the bit cores by an RC discharge. The bit cores containing "ones" put out a pulse that triggers a silicon controlled rectifier (SCR), which latches on and lights a corresponding miniature bulb. Feedback from the lamp circuit puts the "one" back into the proper bit core, thus giving "nondestructive" readout.

When the set-in time has expired, the 10-hr ring emits a pulse that feeds back into the 5-min safety circuit, and if this pulse occurs after 5 min, the firing circuit is pulsed. The firing circuit is a silicon controlled rectifier capable of delivering 2 amp at 6 v.

2. OSCILLATOR DESIGN

A 100.1-cps unijunction transistor oscillator (ref 1) was chosen as the time base. The low frequency was dictated by power consideration. A survey of low-frequency oscillator types indicated that an oscillator built around a unijunction transistor could be designed into 1 in.^{3}, have a frequency in the 100-cps range, and be made stable to better than ±1 percent over the temperature and voltage range (ref 2).

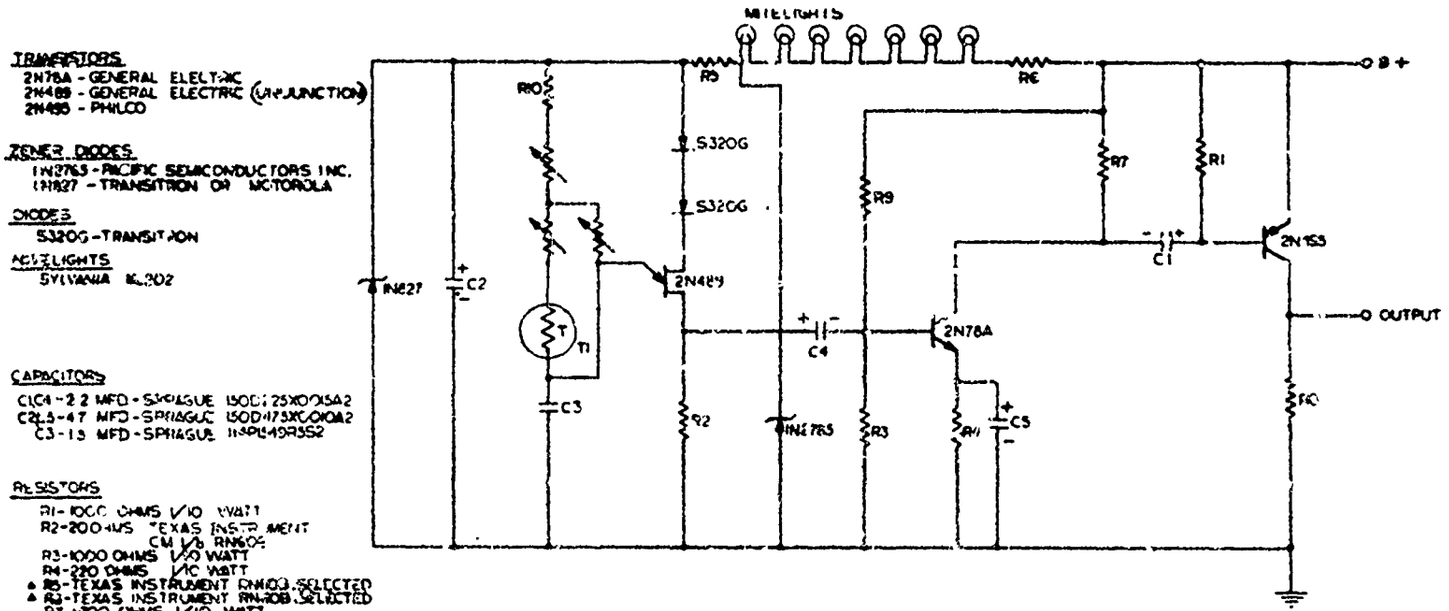
Two 100.1-cps oscillators were built. The first was within ±0.5 percent over the temperature and voltage range. The second was within ±0.25 percent. The temperature range was -55C to +75C and the voltage range was 10.8 v down to 8.4 v. At 10.8 v the oscillator required 18 ma, and at 8.4 it took 11 ma.

The oscillator is composed of three sections: a voltage regulator, a time base determining section, and a buffer amplifier section (fig. 2).

The voltage regulator is composed of a coarse regulator (R6, 7 miniature lamps, 1N2765) and a fine regulator (R5, C2, 1N827).

R5 and R6 are determined as follows:

(a) With 6.5 ma going through the 1N827, the voltage across the 1N827 is recorded to the nearest 0.01 v.



TRANSISTORS
2N78A - GENERAL ELECTRIC
2N489 - GENERAL ELECTRIC (UNIJUNCTION)
2N490 - PHILCO

ZENER DIODES
1N2763 - PACIFIC SEMICONDUCTORS INC.
1N827 - TRANSITRON OR MOTOROLA

DIODES
S320G - TRANSITRON

MINILIGHTS
SYLVANIA ML302

CAPACITORS
C1,C4 - 2.2 MFD - SPRAGUE 150D225X0015A2
C2,C5 - 4.7 MFD - SPRAGUE 150D475X0020A2
C3 - 1.5 MFD - SPRAGUE 150P15R5S2

RESISTORS
R1 - 1000 OHMS 1/10 WATT
R2 - 200 OHMS TEXAS INSTRUMENT CM 1/8 RN60S
R3 - 1000 OHMS 1/10 WATT
R4 - 220 OHMS 1/10 WATT
▲ R5 - TEXAS INSTRUMENT RN60D SELECTED
▲ R6 - TEXAS INSTRUMENT RN60B SELECTED
R7 - 4700 OHMS 1/10 WATT
R8 - 20,000 OHMS 1/10 WATT
▲ R9 - TEXAS INSTRUMENT RN60A, SELECTED
▲ R10 - SELECTED

POTENTIOMETERS
MINELCO MINIATURE ELECTRONICS CORP TYPE PC2
SELECTED FOR TEMPERATURE COMPENSATION (SEE DESIGN PROCEDURE)

THERMISTOR
GULTON INDUSTRIES
SELECTED FOR TEMPERATURE COMPENSATION (SEE DESIGN PROCEDURE)

BOARD NO. 1

▲ SEE DESIGN PROCEDURE

Figure 2. Unijunction transistor oscillator

(b) With 3 ma going through the 1N2765, the voltage across the 1N2765 is recorded to the nearest 0.01 v.

(c) $$R_5 = \frac{V_{1N2765} - V_{1N827}}{0.0075}$$

(d) R_6 is determined by adjustment until the voltage across the 1N2765 equals V_{1N2765} with 3.4 v across the network. C_2 is used for filtering since the time base section requires different levels of current during a cycle. The seven miniature lamps are used to reduce the current consumption of the regulator at the upper voltage limit, since the resistance of the lamps increases with an increase in current. The lamps also aid in stabilization since any increase in current also means a change of voltage level of the Zener diode.

$$\Delta i \times \Delta R = \Delta V,$$

where ΔR is the dynamic impedance of the Zener. Use of the lamps compared with a fixed resistor decreases the voltage spread across the 1N827 by a factor of two.

Typical performance data of the regulator are given:

Temp (C)	V_{in} [a] (v)	V_{course} [b] (v)	V_{fine} [c] (v)	I_{ma} [d] (ma)
-55	8.4	6.83	6.285	12.5
-55	10.8	6.89	6.30	18.5
30	8.4	6.83	6.29	11.0
30	10.8	6.93	6.31	17.0
75	8.4	6.83	6.29	10.7
75	10.8	6.94	6.31	17.0

[a] V_{in} is the voltage across the regulator.

[b] V_{course} is the voltage across the 1N2765.

[c] V_{fine} is the voltage across the 1N827; this voltage is the voltage which appears across the time base portion of the oscillator.

[d] I_{ma} is the current drawn by the regulator and the time base section only.

The time base determining section is composed of an 2N489 unijunction transistor, a resistance-capacitor combination (R_{10}, three potentiometers, a thermistor, and C_3); two S320G stabistors; and R_2, the output resistor. The oscillator is basically a relaxation-type device. Voltage builds up across C_3 to the triggering point of the 2N489. C_3 is then discharged into R_2. The stabistors are used to change the triggering point temperature characteristics of the unijunction transistor (fig. 3). The two-stabistor curve was determined best for the overall oscillator since it allowed compensation of the resistance in the resistance-capacitor network with a thermistor. C_3 is a polystyrene capacitor with excellent stability and a linear temperature coefficient of -120 ppm. R_{10} is a wire-wound resistor.

The entire oscillator, except the three potentiometers and the thermistor, was subjected to temperature cycling, and at 10° C intervals the value of resistance needed to make the oscillator frequency 100.1 cps was determined. This value was to be matched by the network of the three potentiometers and the thermistor. Also, the resistances of a number of thermistors were determined as functions of temperature. Proper values of the three potentiometers were determined by means of an IBM704 computer. (See reference 3 for a summary of the program.) The information furnished the computer was a table of resistance-versus-temperature readings for the oscillator to be exactly on frequency, and a table of resistances versus temperature for several different thermistors. The computer then used this information to determine the best settings of the three potentiometers and the best thermistor to be used to give the smallest percentage of deviation over the temperature range. The three potentiometers are wire wound with temperature coefficients of 0 ± 10 ppm. In addition, the computer predicted the error at each temperature after compensation. The maximum error predicted was ±0.1 percent. Actual results, however, were ±0.25 percent and ±0.3 percent (appendix A). These discrepancies are attributed to the inaccuracy of the initial resistance readings. It is believed that the 0.1 percent could be obtained with a more accurate resistance substitution box (0.1 percent of its highest reading). Since R_{10} is at least 80 percent of R(R is composed of the three potentiometers and the thermistors; R_{10} is in the temperature chamber) and the period is proportional to the $(R_{10} + R)C_3$ product, then having data for R to ± 0.1 percent is equivalent to adjusting the frequency accurately to 0.02 percent. With data this accurate, it would be expected that the oscillator could be made accurate to ± 0.1 percent or better.

The output waveform across R_2 is seen in figure 4. Since the output voltage and wave shape was not optimum to trigger the core driver, a buffer amplifier had to be used. The buffer is a two-stage

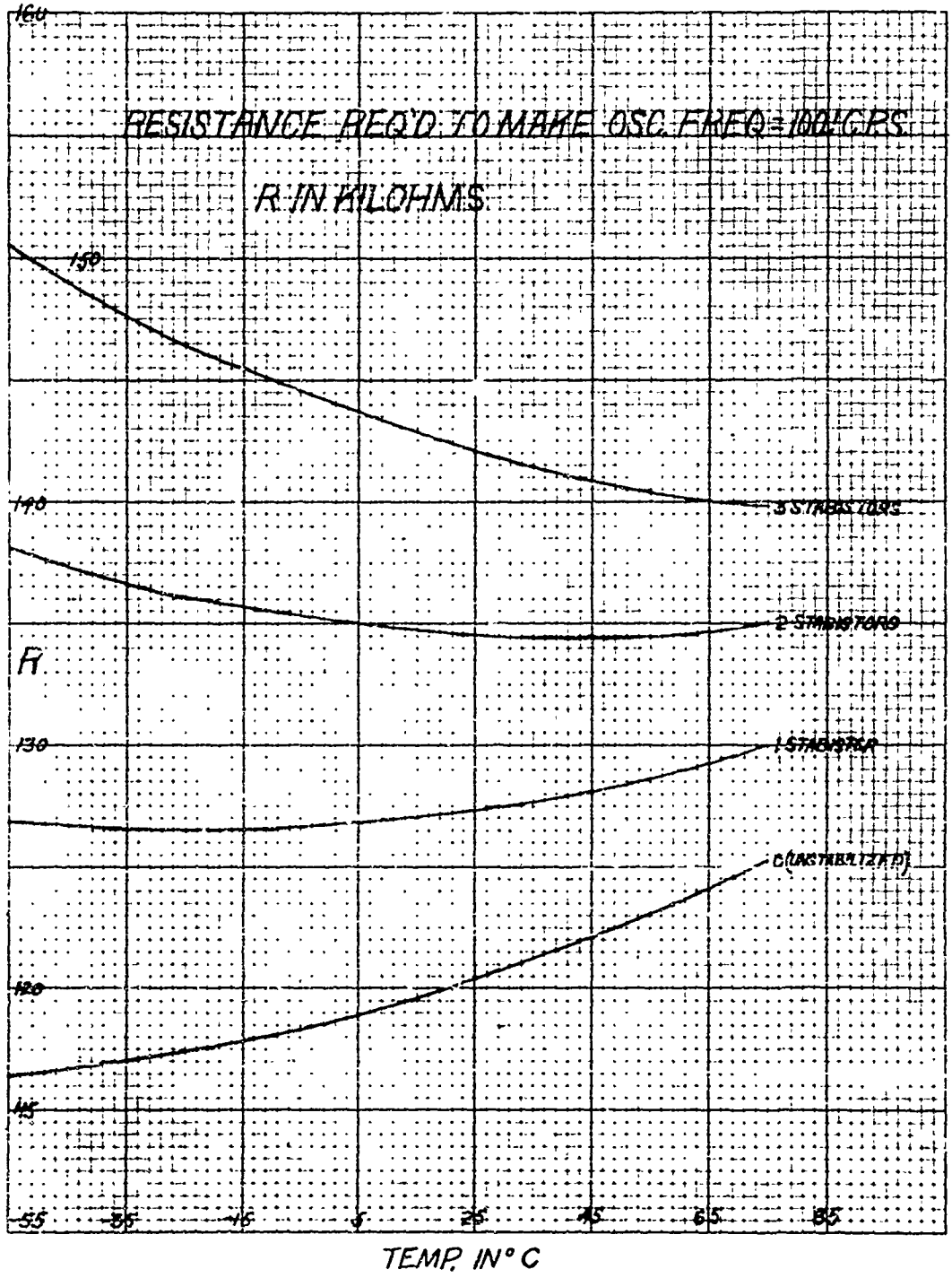
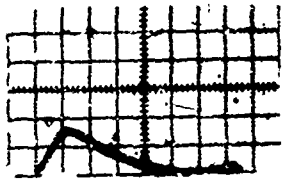


Figure 3. Resistance required to make oscillator frequency 100.1 cps

1

HOR 5μs/cm Vert 0.5v/cm



Oscillator Output

2

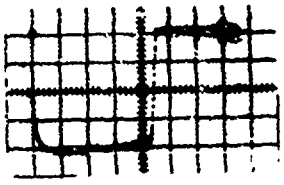
HOR 5μs/cm Vert 100 ma/cm

Drive Pulse T_1

(Across 1 ohm inserted in drive T_1 line when setting)

3

HOR 5μs/cm Vert 100 ma/cm



Drive Pulse T_2

(Across 1 ohn inserted in drive T_2 line when setting)

Figure 4. Wave forms 1755-61

RC coupled amplifier with the first stage biased on. The forward bias is required since the output of the oscillator is not enough to overcome the base-to-emitter voltage of the 2N78A at low temperatures. R_9 is used to provide the bias, and it is selected as follows:

(a) At room temperature with R_9 left out and with 9.6 v applied to the oscillator the total current drawn by the oscillator is determined.

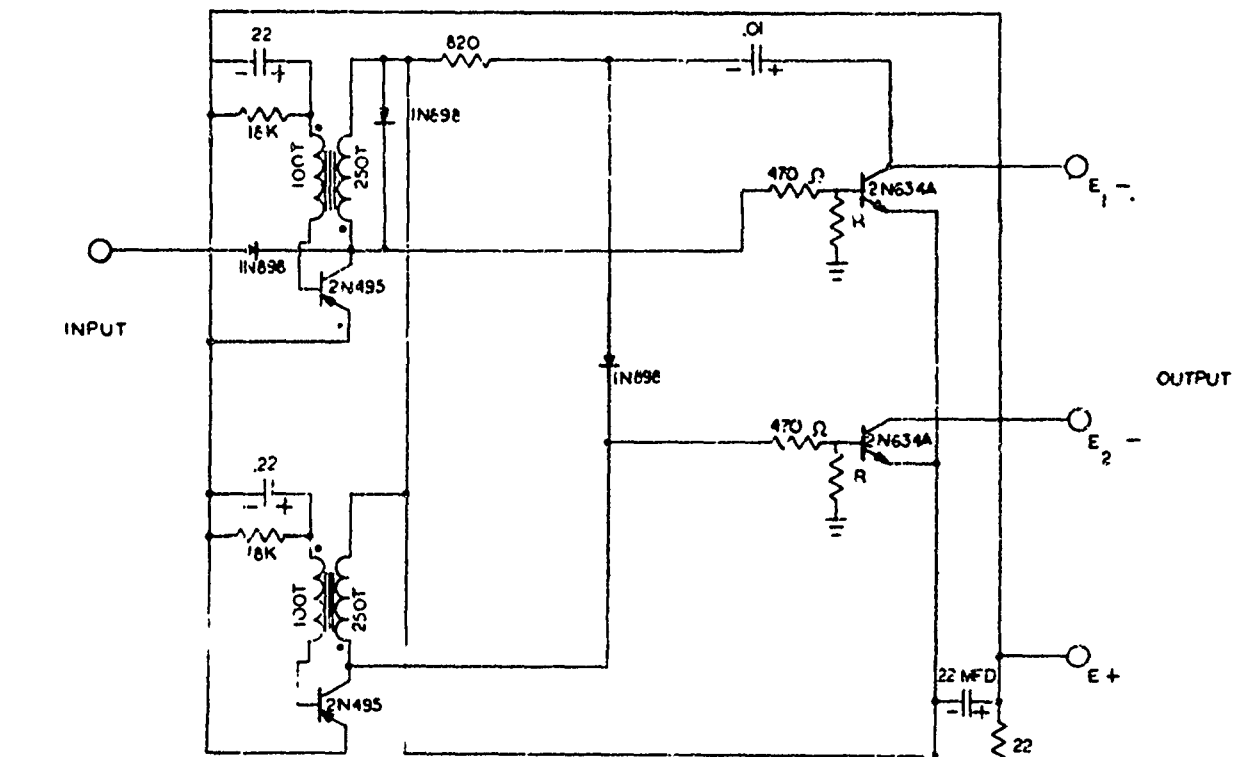
(b) A resistance box is substituted for R_9 and the resistance is changed until the current increases by 0.5 ma ± 10 percent. This resistance value is used for R_9.

Nine such buffers were built and in all cases R_9 was 56 kohms. However, other lots of 2N78A transistors with different gains may require different values of R_9. An alternate method that can be used is to have a fixed R_9 and to specify the gain of the 2N78A.

The output waveform to the core driver is a square pulse close to B+ in value and between 10 to 12 μsec in width. The current drawn by the buffer stage is essentially the 0.5-ma bias current.

3. CORE DRIVERS

The core diode shift registers described in section 4 are of the two-core per bit variety. These shift registers are driven by two successive current pulses, and thus the driver requirement is to provide two sequential current pulses on separate lines about 30 μsec wide at approximately 400 ma. This requirement is accomplished by having the oscillator pulses trigger a blocking oscillator whose pulse width is 30 μsec. This pulse then is fed to 2N634A amplifiers that supply the current pulses to the cores (fig. 5). The second current pulse is generated by having a differentiating network across the 2N634A that puts out a positive pulse when the current pulse of the 2N634A shuts off. This positive pulse triggers another blocking oscillator that drives a second 2N634A, and thus gives the second current pulse. The 18-kohm resistor and the 0.22-μf capacitor in the base circuit of the 2N495 determine the blocking oscillator pulse width. The charging of the capacitor causes shutoff. The RC discharge of the 0.22-μf capacitor into the 18-kohm resistor holds the blocking oscillator off for a long enough time so that it may not be driven faster than about 120 cps. This insures against catastrophic short times that could occur if the oscillator frequency were suddenly increased. If the 18-kohm and 0.22-μf combination is shorted out, the blocking oscillator shutoff is accomplished by saturating the core, and the pulse width is slightly longer than before. The 22-μf capacitor is used to reduce the peak current requirements from the battery. These pulses are constant current pulses since the amplifiers are never saturated (fig. 4). The value of the current is adjusted by choosing the proper value of R.



PHILCO TRANSISTOR-2N495
GENERAL ELECTRIC TRANSISTOR-2N634A
TOROIDAL CORE (GENERAL CERAMIC NO. F-625 TYPE Q)
COIL TURNS AS INDICATED WIRE SIZE AWG. 38 FORMVAR
PACFIC SEMICONDUCTOR DIODE - IN698
ALL RESISTORS ARE 1/2 WATT
CAPACITORS ARE SPRAGUE - TANTALEX -
.01 - 150D103X0035A2
.22 - 150D224X0035A2
22 MFD - 150D226X0015B2
FOR THE VALUE OF "R" SEE DESIGN PROCEDURE

Figure 5. Single amplifier driver

The value of R varies since the gain differs from transistor to transistor. Figure 6 shows the driver used for the 30,030 divider. Two amplifiers are required for each pulse, since the resistance of the number of cores that are required to be switched at one time is too great for the voltage used. A single amplifier would be driven into saturation and its constant current function destroyed. Thus two amplifiers are used in parallel, each operating unsaturated. The adjusted value of R is such that with 11 v on the driver, at room temperature, the current is adjusted to 425 ma. Values of R greater than 200 ohms are not used since they would cause high leakage of the amplifier at high temperature. If adjustment shows that the required R is greater than 200 ohms, the resistor from the collector of the 2N495 to the base of the 2N634A may be reduced slightly but not enough to load the blocking oscillator. If no such compromise can be made the transistor is replaced with one having a higher gain. Here, again, adjustment may be eliminated by rigid specifications of the 2N634A.

The four current pulses that drive the 30,030 divider are adjusted to within ±2 percent of each other. The drivers used for the three serial shift registers do not require close matching and are adjusted to 425 ma ±10 percent. Variations in the value of the battery voltage cause corresponding variations in the current pulses. With the drivers set by the preceding procedure, the timer will work over battery voltage variations of 11 v to 8.4 v. Greater range would be achieved with the incorporation of a Zener diode and a resistor in the blocking oscillator circuits with no additional power losses. It should be noted that the first driver has a duty cycle of less than 0.5 percent and subsequent drivers have much smaller duty cycles.

4. THE SINGLE-DIODE LOOP AND THE SHIFT REGISTER

The magnetic cores used as the basic element of the shift registers are 4-79 molybdenum permalloy tape-wound cores. This material was chosen because its magnetic properties change very little with temperature. The cores have a hysteresis loop similar to the one in figure 7. The abscissa corresponds to drive in ampere turns while the ordinate is flux in maxwells. The same type of core was used in all the shift registers. The cores are driven so as to be either in the "one" state or in the "zero" state. Figure 7 presents a summary of the polarity conventions used throughout this paper.

Figure 8 shows a single-diode loop. The single-diode loop is the basic circuit element used in all the shift registers and the AND circuits. Information is transferred from core to core as outlined below. Assume core A is in the "one" state and core B is in the "zero" state. Drive current at time T_1 flows through coil N_o of core A and drives core A toward the "zero" state. A voltage is induced in winding N_1 of core A, causing current to flow through coil N_2 on core B. This current drives core B toward the "one" state. Information is switched

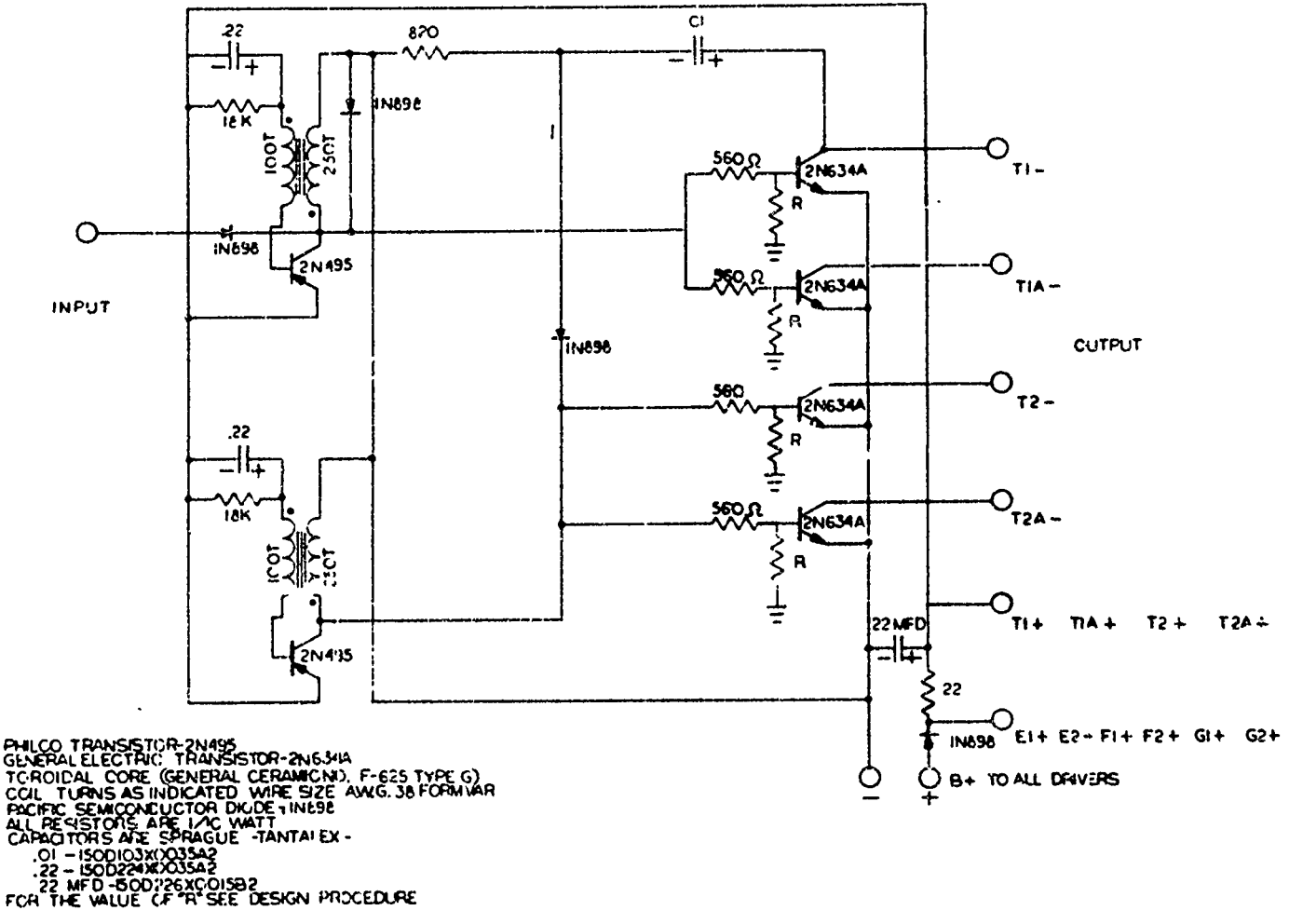
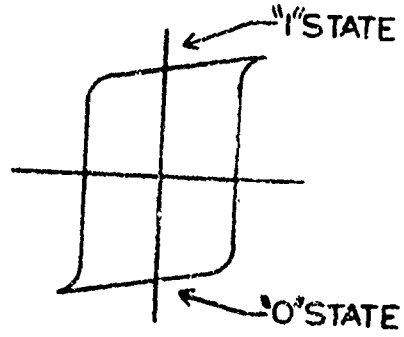
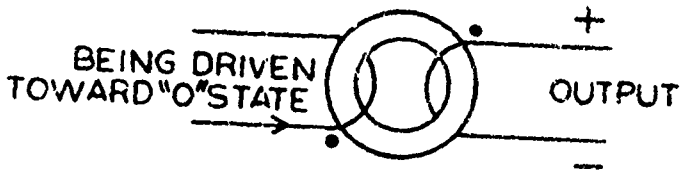


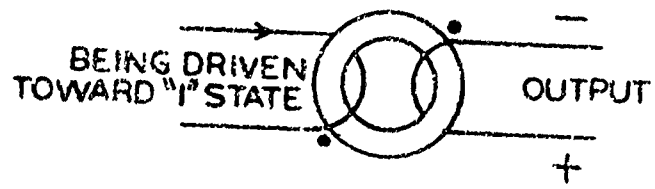
Figure 6. Double amplifier driver



HYSTERESIS LOOP



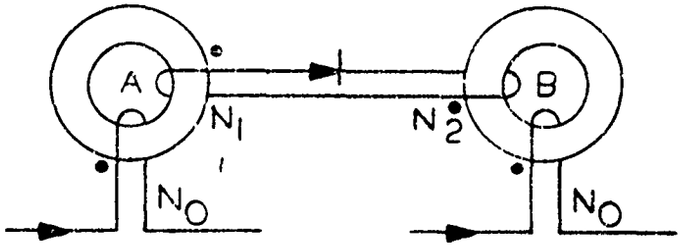
INITIALLY IN "1" STATE



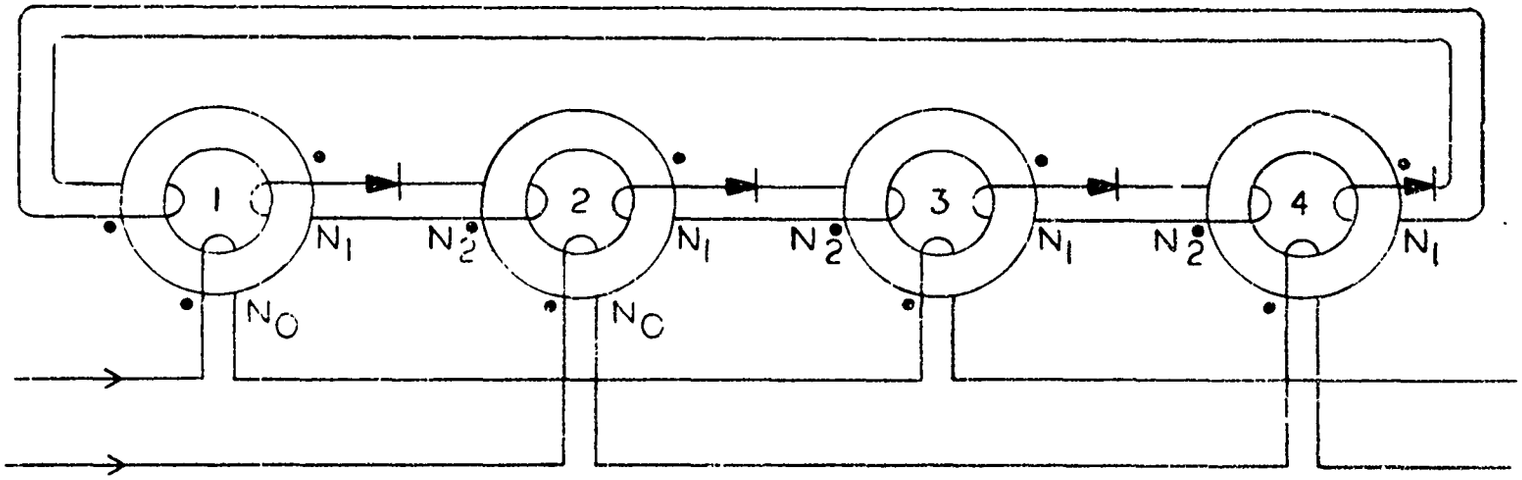
INITIALLY IN "0" STATE

CORE CONVENTIONS

Figure 7. Hysteresis loop and magnetic core conventions



SINGLE DIODE LOOP



2 STAGE SHIFT REGISTER

Figure 8. Single-diode loop and two-stage counter

out of core B to the following core by a similar sequence. Drive pulse T_2 flows through coil N_o of core B and drives it toward the "zero" state. Winding N_1 on core B (not shown) allows current to flow to the next loop. However, it is noticed that winding N_2 on core B also induces a voltage, causing current to flow back toward core A. This current, however, is low because the number of turns on coil N_2 is smaller than the number of turns on coil N_1, and thus a lower voltage is induced than that in the forward direction. The voltage drop across the diode also reduces this back current, so that core A will not switch. The worst case design procedure used for these loops is developed in reference 3. Figure 8 shows the wiring of a 2-stage shift register. Assuming core 1 is in the "one" state and cores 2, 3, and 4 are in the "zero" states and assuming an output is taken across coil N_1 of core 4, the sequence is as follows:

Oscillator Pulse No.	Drive Pulse	Location of Bit Before Drive Core No.		Location of Bit After Drive Core No.
O - Before Oscillator Starts	-	1		1
1	T_1	1		2
	T_2	2		3
2	T_1	3		4
	T_2	4	Output	1
3	T_1	1		2
	T_2	2		3
4	T_1	3		4
	T_2	4	Output	1

Division by two is accomplished. By adding additional stages, division by higher integers is possible. In the 30,030 section, four shift registers of 11, 13, 14, and 15 stages are used. In the time settable ring counter section, three shift registers of 12, 10 and 6 stages are used.

5. THE 30,030 DIVIDER

Division by the 30,030 divider (fig. 9 and 10) is accomplished by combining with AND circuits the output of four shift registers having 11, 13, 14 and 15 stages. These numbers are relatively prime to one another and thus only once every 11 x 13 x 14 x 15 (30,030) times is there simultaneous output from the output cores of these shift registers. Since the oscillator frequency is 100.1 cps, the output frequency of the divider is one pulse every 5 min.

The AND function is accomplished in three steps. First, the 11- and 13-stage outputs are combined so that core AN1 has an output once every 143 clock pulses. Second, the 14- and 15-stage outputs are combined so that core AN2 has an output once every 210 clock pulses. Third, the outputs of cores AN1 and AN2 are combined in core AN3 which gives one output pulse for every 30,030 input clock pulses.

The AND operation is as follows: Each of the cores A22, B26, C28, D30 of ring counters A, B, C, and D not only drive the following core in its own ring, but each drives in addition core AN1 or AN2. All these inputs tend to drive AN1 and AN2 toward the "one" state. Cores AN1A and AN2B tend to drive cores AN1 and AN2, respectively, toward the "zero" state with each clock pulse. Consider AN1. If both A22 and B26 do not shift a "one" into AN1, AN1 does not go into the "one" state. If either A22 or B26 tries to shift a "one" into AN1 core, the drive of AN1A's bucks it out equally. However, if both A22 and B26 drive AN1 toward the "one" state it will go into the "one" state since core AN1A can only buck out one of the inputs. Similarly, core AN2B tries to buck inputs by C28 and D30 into core AN2. For bucking action to be complete the pulses must match in amplitude and duration. To do this the drive currents $\overline{I}_1$, $\overline{I}_1A$ and $\overline{I}_2$, $\overline{I}_2A$ are set as close as possible as described in section 3. In addition, core AN1A is made to drive idler core AN1B and core AN2B is made to drive idler core AN2A. These two idler cores match the shift register cores that are driven by A22, B26, C28, and D30. Similar AND operation is accomplished in core AN3 where the input cores AN1 and AN2 are being bucked out by core AN3A.

The output of AN3 is one pulse every 5 min. This output is used to put a "one" into the AN3B and the "5-min" cores. The purpose of the "5-min" core is explained in section 8. This core is initially set in the "zero" state and gets driven toward the "one" state after 5 min. The purpose of core AN3B is also explained in the section 8. Core AN3B is initially set in the "one" state and gives out an output on the first clock pulse. Figures 11 and 12 show oscillographs of the waveforms at pertinent points.

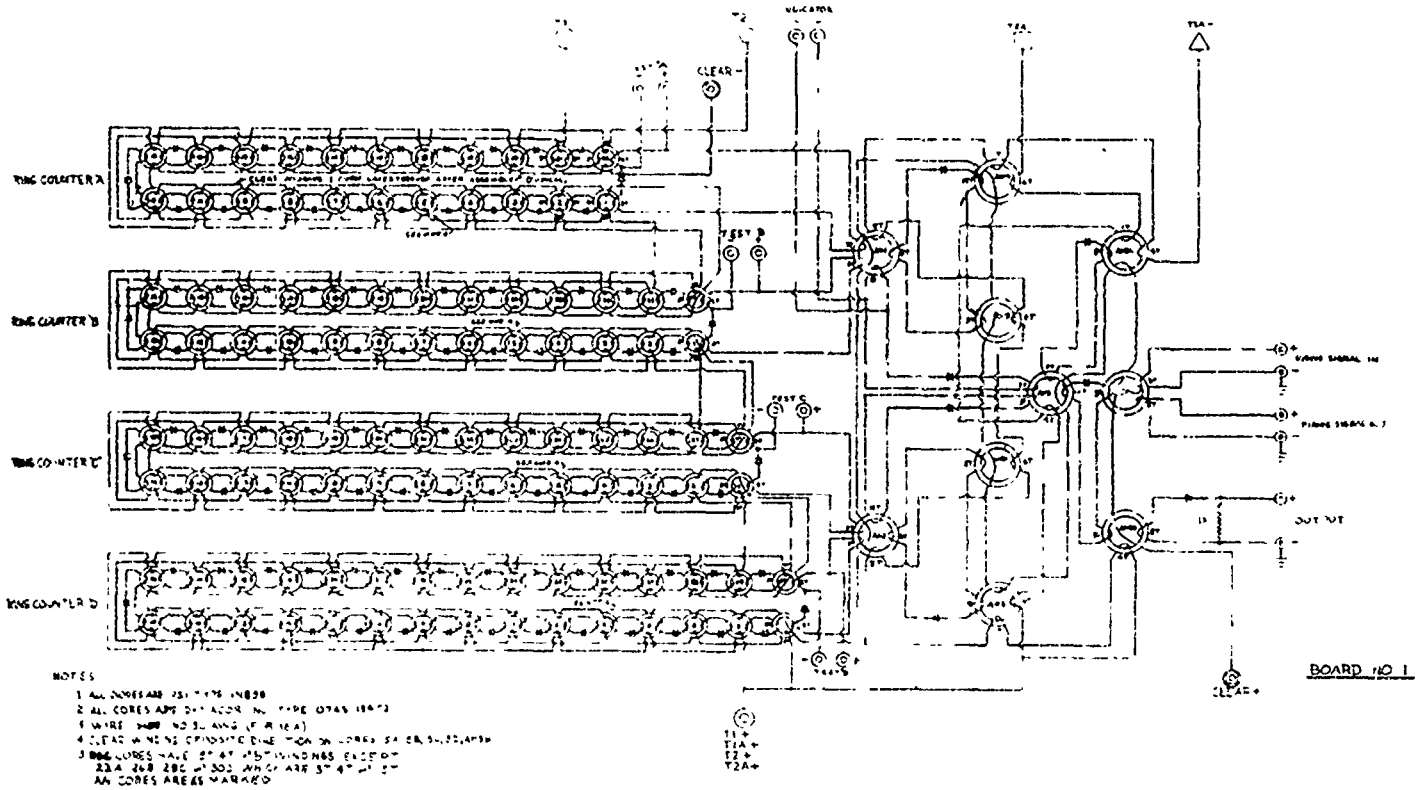


Figure 9. 30,030 divider

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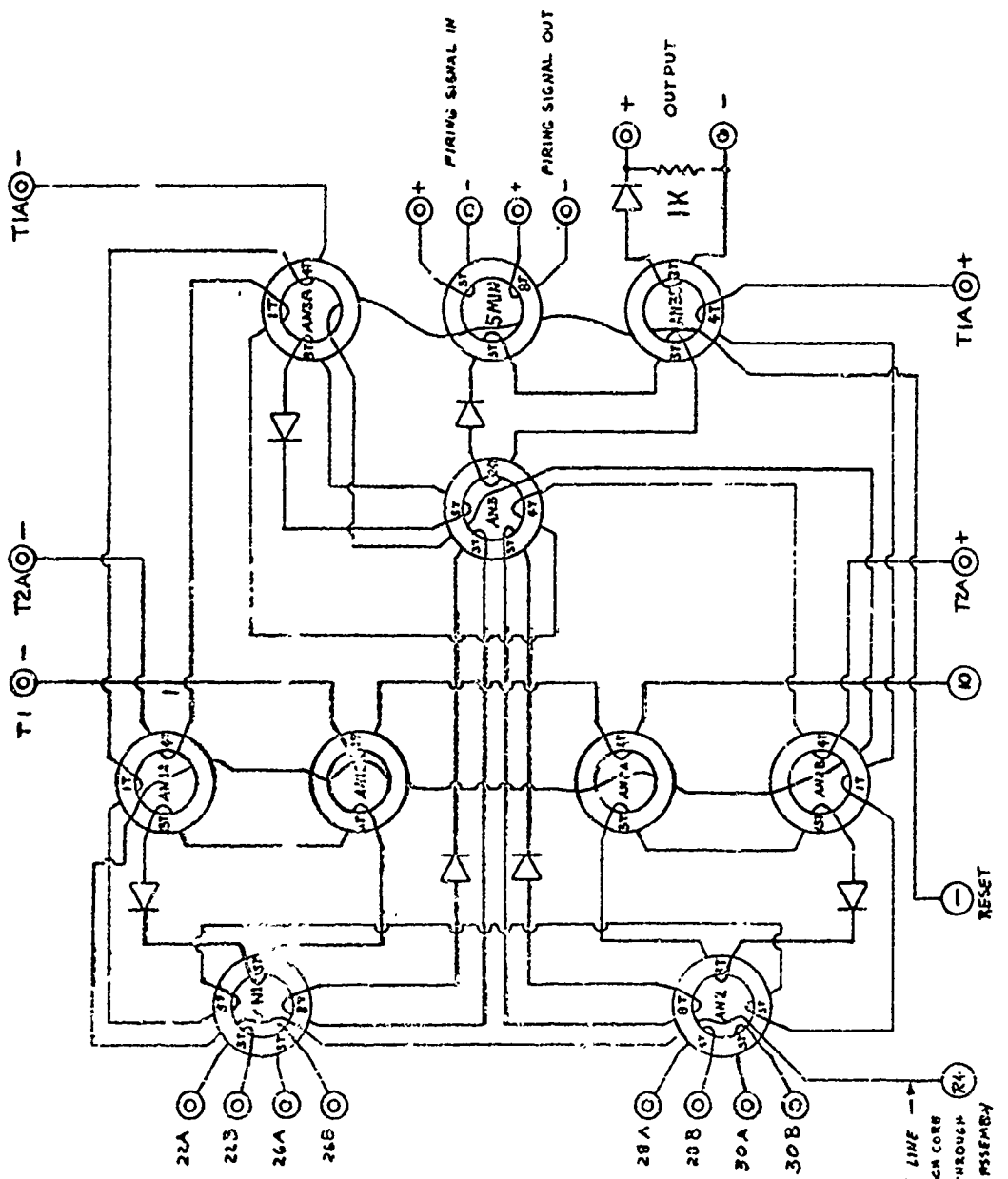
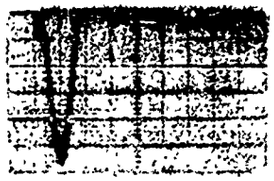


Figure 10. AND circuit

1

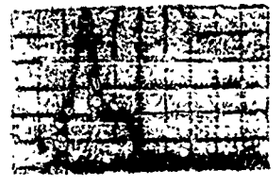
HOR 2μs/cm Vert 1 v/cm
CORE A3 8 Turn Winding



"0" to "1"

2

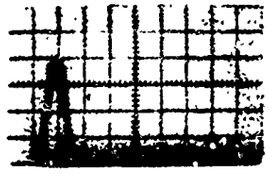
HOR 2μs/cm Vert 0.5 v/cm
CORE A3 8 Turn Winding



"1" to "0" (large pulse)
"0" to "0" (small pulse)

3

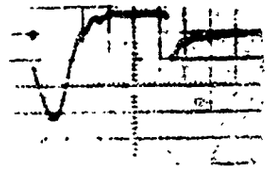
HOR 2μs/cm Vert 0.5 v/cm
CORE A4 3 Turn Winding



"0" to "1"

4

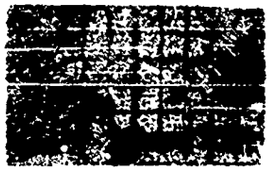
HOR 2μs/cm Vert 1 v/cm
CORE AN1 8 Turn Winding



"0" to "1"
(1 pulse / 1.43 sec)

5

HOR 2μs/cm Vert 0.5 v/cm
CORE AN1 8 Turn Winding



"1" to "0"
(1 pulse / 1.43 sec)

6

HOR 2μs/cm Vert 1 v/cm
CORE AN1 8 Turn Winding

"1" to "0"
(1 pulse / 5 minutes)

Figure 11. Wave forms 1757-61

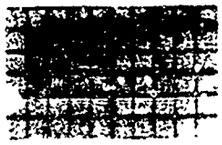
7

HOR 5μs/cm Vert 0.5 v/cm
CORE AB3 24 Turn Winding

"1" to "0"
(1 pulse / 5 minutes)

8

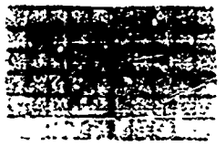
HOR 5μs/cm Vert 5 v/cm
CORE AB3 24 Turn Winding



"0" to "1"
(1 pulse / 5 minutes)

9

HOR 1 μs/cm Vert 5 v/cm



"0" to "1"
(1 pulse / 5 minutes)

10

HOR 1 us/cm Vert 0.5 v/cm
CORE C25 4 Turn Winding

"1" to "0" (large pulse)
"0" to "0" (small pulse)

11

HOR 1μs/cm Vert 5 v/cm
CORE AB3B 8 Turn Winding

"0" to "1"

12

HOR 2μs/cm Vert 1 v/cm
CORE AB3B 8 Turn Winding

"1" to "0"

13

Shift Register A

/0000000000/0
Division by 11

Figure 12. Wave forms

1756-61

6. THE MONITOR CIRCUIT

The basic purpose of the monitor circuit is to be able to have a visible indication that the timer is operating when it is in the ON position. It also serves as a rough indication of the timing accuracy. The circuit is basically a one-shot multivibrator. Its input is derived from the output of core AN1. It thus is pulsed about once every 1.43 sec. It is so designed that the lamp is pulsed off. The input of 260 ohms is required so that the AND circuit will not be loaded down (fig. 13). The diode limits current from flowing back into the AND circuit. The input 2N703 is pulsed on and the other two 2N703's then stop conducting and the lamp is extinguished. The off time is controlled by the 2.2-μf condenser and the 220-kohm resistor. Since the 220-kohm resistor also limits the base current into the middle 2N703, it thus controls the maximum collector current. Due to the long shutoff time required, the high value of 220 kohms was needed. The last 2N703 is used as an amplifier to supply the 30-ma I_C required for the lamp. The 4700-ohm resistors connected to the base of the 2N703 are used for regeneration. The monitor circuit indicates operation of the oscillator, the first drive, the 11- and 13-stage shift registers, and part of the AND circuit.

7. THE THREE SERIAL SETTABLE COUNTERS

Figure 14 shows the three serial settable shift registers. Each shift register contains one "one" in it. The output of the 30,030 divider pulses the E driver that supplies the shift pulses for the 12-stage shift register. The "one" in this register moves from stage to stage in 5-min steps. The output of this shift register pulses the F driver that supplies the shift pulses for the 10-stage shift register. Here the shifting takes place once every hour. The output of this register pulses the G driver that supplies the shift pulses for the 5-stage register. Here the shifting takes place once every 10 hr. The output of the 5-stage shift register is the firing signal. This pulse is fed back into the "5-min" core of the 30,030 divider. The purpose of this is clarified in section 8. The 5-stage shift register is not a complete ring, as were all the other shift registers, since this shift register supplies the firing pulse and no further counting is required after this time.

8. THE CLEAR AND SET, KICKDOWN, AND FIVE-MINUTE SAFETY

The clearing and setting of all the bistable magnetic cores are done at once. The mechanism for setting a core into a desired state is simply to pulse the core with a high-current pulse. The desired state is achieved by using the conventions outlined in figure 7. An RC discharge is run through the single turn winding connecting all the cores.

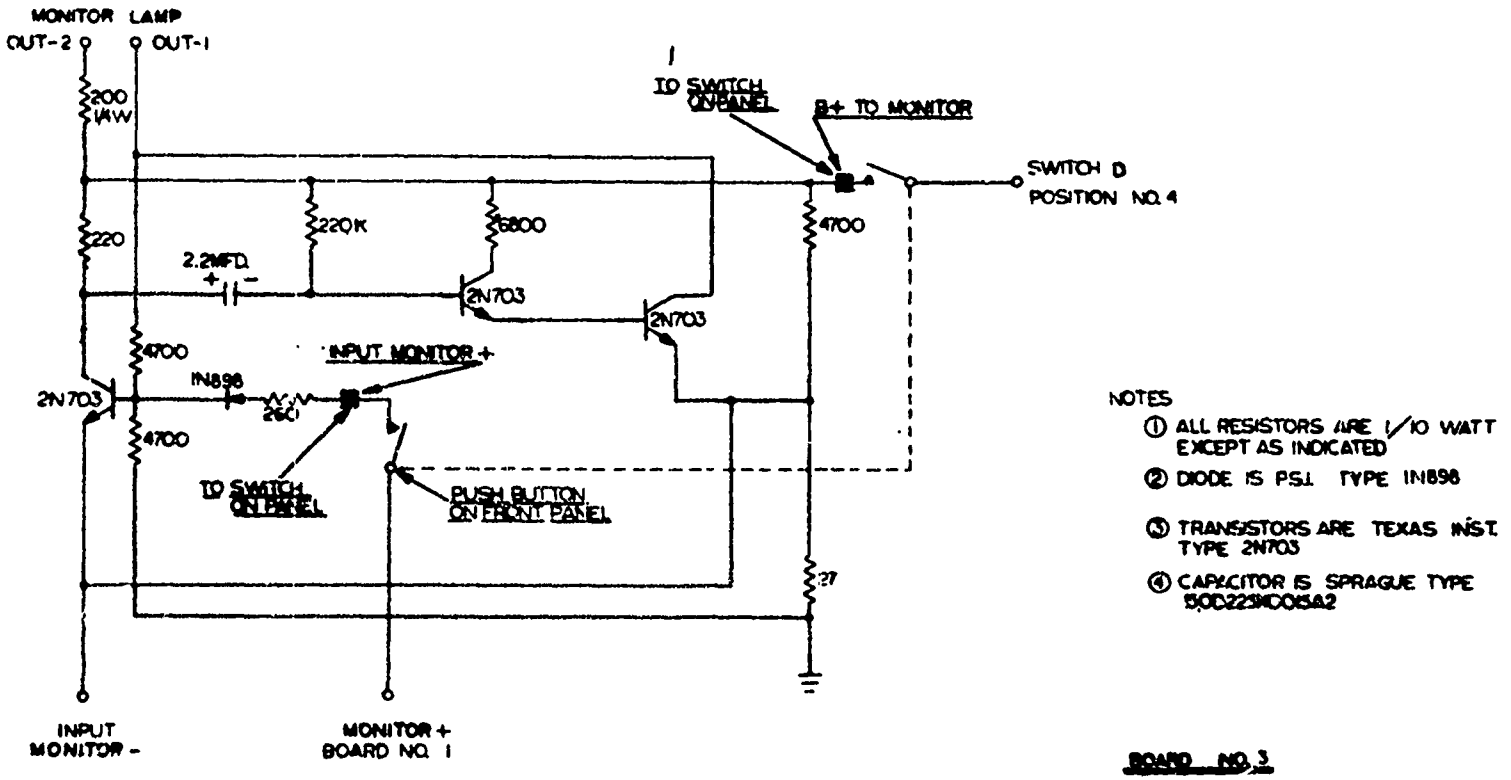


Figure 13. Monitor circuit

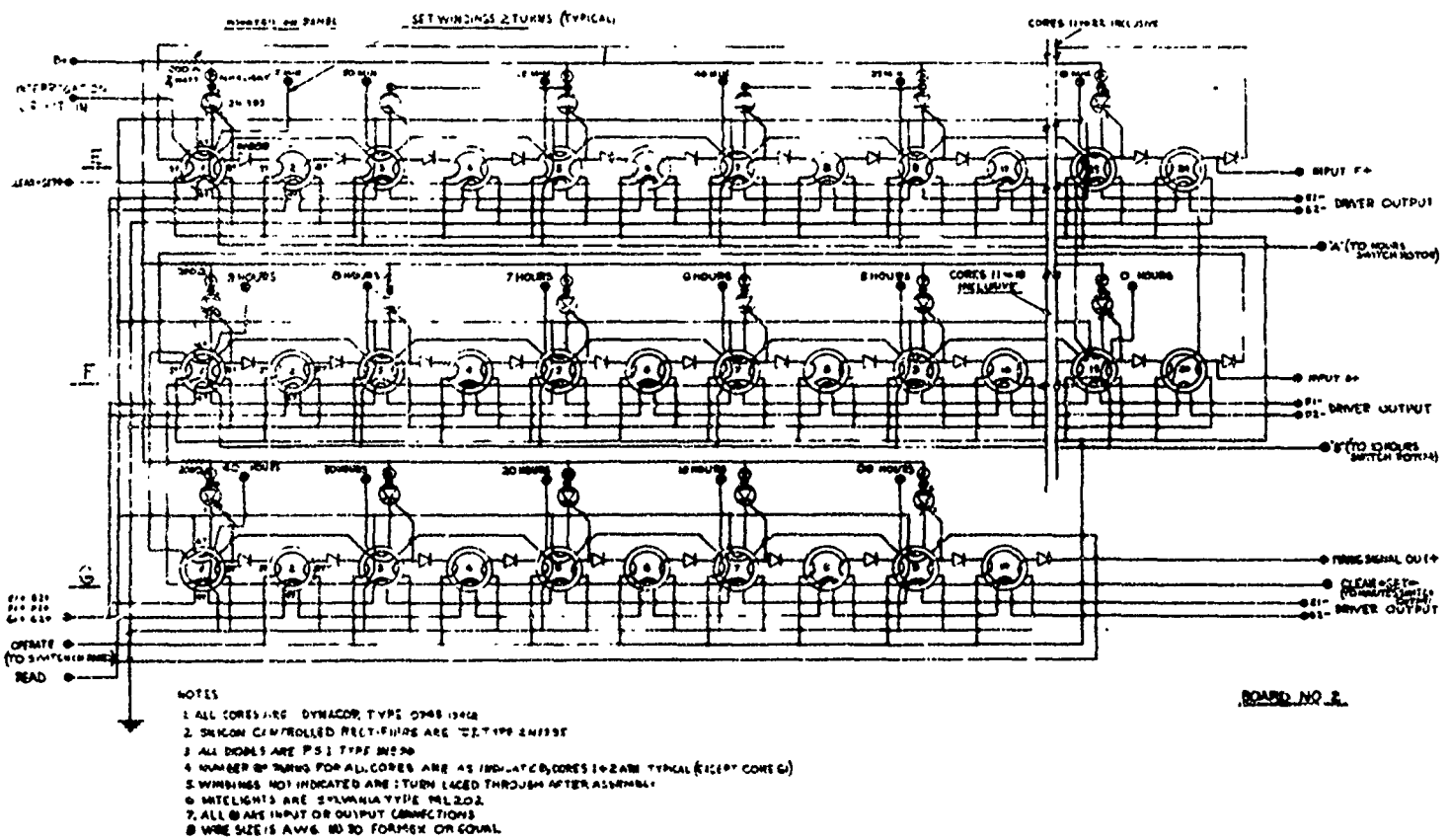


Figure 14. Three serial settable counters

To set the desired function time, three cores in the three serial settable shift registers must be set. One "one" must be put in each register. The principle used is illustrated in figure 15. It is seen that the clear winding tends to drive all the cores in these three registers toward the "zero" state. However, through the three time-setting switches the cores chosen to be set have their two-turn set windings placed in series with the clear winding. Thus, each selected core has one net turn driving it toward the "one" state. This method has the advantage of combining the clearing and setting into one operation and insures that only one combination of three "ones" is set into the registers. It should be noted that the clear winding puts the "one" into the 11-, 13-, 14-, and 15-stage registers of the 30,030 divider in the third stage. This is because it takes two clock pulses to perform the AND operation and, if the registers were set in the first stage, the first 5-min pulse would arrive two clock pulses or 0.02 sec late.

Each stage of the three settable shift registers is labeled according to its time set function, thus the 12-stage register has its stages labeled as follows: 55 50 45 40 35 30 25 20 15 10 5 0, where the "one" is shifted from the 55-min core toward the 0 core. When the 0 core is shifted the "one" is returned back to the 55-min core, the carry takes place, and the hour shift register is pulsed one step. The hours register has its cores labeled 9 8 7 6 5 4 3 2 0. It, too, carries when the shift takes place from 0 hr to 9 hr. The 10-hr shift register has its cores labeled 40 30 20 10 00. The firing signal takes place when the 00 core has its "one" shifted out.

Assume that the cores were set so that a "one" was placed in the 00-hr core, the 0-hr-core, and the 5-min core. Thus the expected firing time is 5 min. When the function switch is turned from the SET position to the READ position, the lamps corresponding to these cores light (the mechanism for readout is clarified in the section 10), indicating that the firing time is 5 min and verifying the set in time. When the function switch is turned to the ON position, the timing starts since the oscillator is connected into the circuit. The first oscillator pulse trips shift pulse T_{1A}, which is used to drive the AND circuit and core AN3B. Core AN3B was cleared to the "one" state and upon receiving T_{1A} puts a pulse into the input of the three serial settable shift registers. This is called the kickdown pulse. The serial registers now have received their first 5-min pulse but at zero time. This moves the setting to 00 ten hours, 0 hr, and 0 min. However, no firing pulse is given out until 5 min later when all three registers carry and the 00 ten-hours core is shifted out. The purpose of this sequence is so that when the device is read out for the time remaining, it will read out a minimum time. For example, if the counter is set for 23 hr and 20 min and turned ON and then turned to the READ position 17 min later, the time remaining to fire would read 23 hr and 0 min. This indicates a minimum time to fire of 23 hr and 0 min and a maximum time of 23 hr and 5 min.

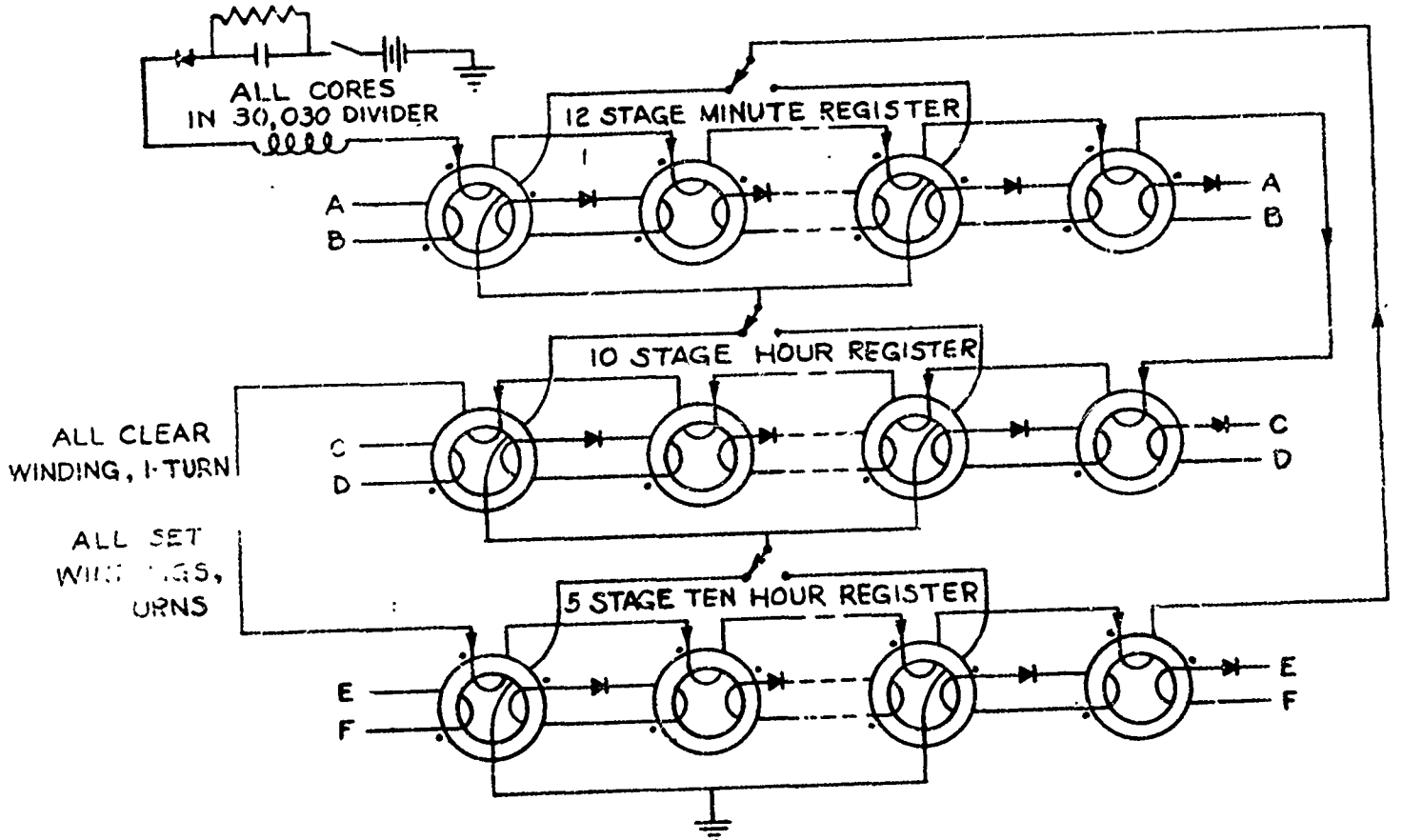


Figure 15. Time set circuit

The 5-min safety feature does not allow functioning if the timer is set for operation at zero time. This is accomplished by taking the firing pulse from the ten-hours register and using it to drive the "5-min" core toward the "zero" state. The "5-min" core is initially cleared into the "zero" state. Core AN3 drives the "5-min" core into the "one" state at five minutes. Thus, if the firing signal comes at or after 5 min the "5-min" core gives out a pulse. Now if the timer is set for 0 time and turned ON, the kickdown pulse immediately has the 00-core shift and drives the "5-min" core toward the "zero" state. Since AN3 has not put a "one" into the "5-min" core, the "5-min" core does not give out an output.

Since the ten-hours register is not a closed register, it will never give out another pulse and thus the timer will not fire unless reset. The output of the "5-min" core delivers the triggering pulse to the firing circuit.

9. FIRING CIRCUIT

The firing circuit in designed around a 2N1595 silicon controlled rectifier (fig. 16). One side of the output is grounded and the other side is connected to the cathode of the SCR. The 1-kohm resistor between the gate and cathode prevents the SCR from spontaneous turn-on when the B+ charge is applied. Particular care must be taken to be certain that this resistor is connected into the circuit and that it is not open. Upon receiving the firing signal from the "5-min" core, the SCR latches on and delivers continuous current to the output load until the output load opens when it activates. The output load is connected to the OUTPUT terminals on the prototype.

10. READOUT

Figure 17 illustrates the "nondestructive" readout principle used. When the function switch is in the read position all the diode loops are open and B+ is applied to the SCR's and the RC interrogate line. This pulse tends to drive all the bit cores toward the "zero" state. Assume core 1 contains a "one" and core 3 contains a "zero." Upon interrogation, core 1 puts out a positive pulse and core 3 puts out a low-noise pulse. Point A goes positive and turns on its corresponding SCR. The signal at point B is well below the threshhold value for its corresponding SCR and it does not turn on. The lamp corresponding to core 1 turns on. Current flows through the SCR and is high enough so the SCR can latch on. Current from the cathode flows through the return winding to ground. This winding is in the direction to return a "one" back into core 1. Thus the core has been read out and the information returned to the core. Core 3 remains in its original "zero" state. When the function switch is turned to the ON position, the B+ is no longer on the SCR's and the lamps extinguish. The loops are closed and the shift registers are restored. The readout operation may be done any number of times.

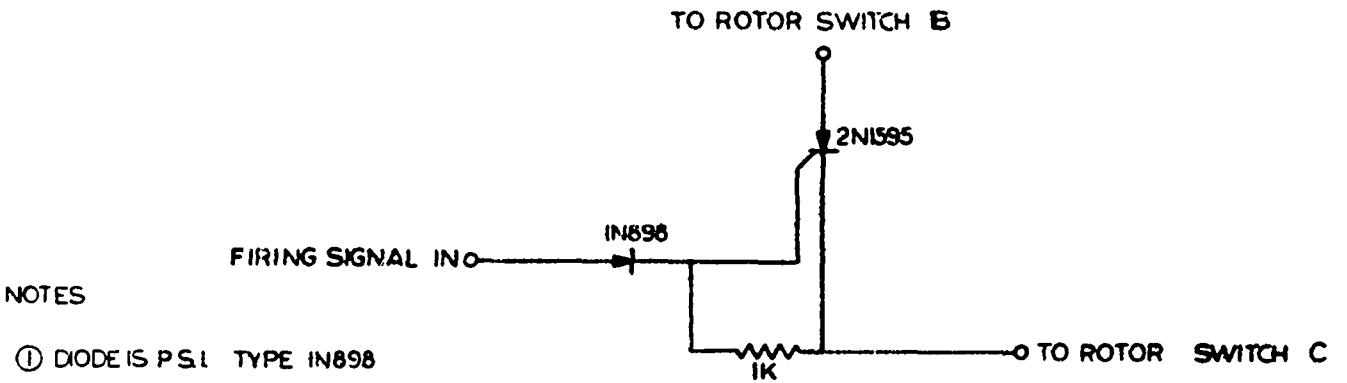


Figure 16. Firing circuit

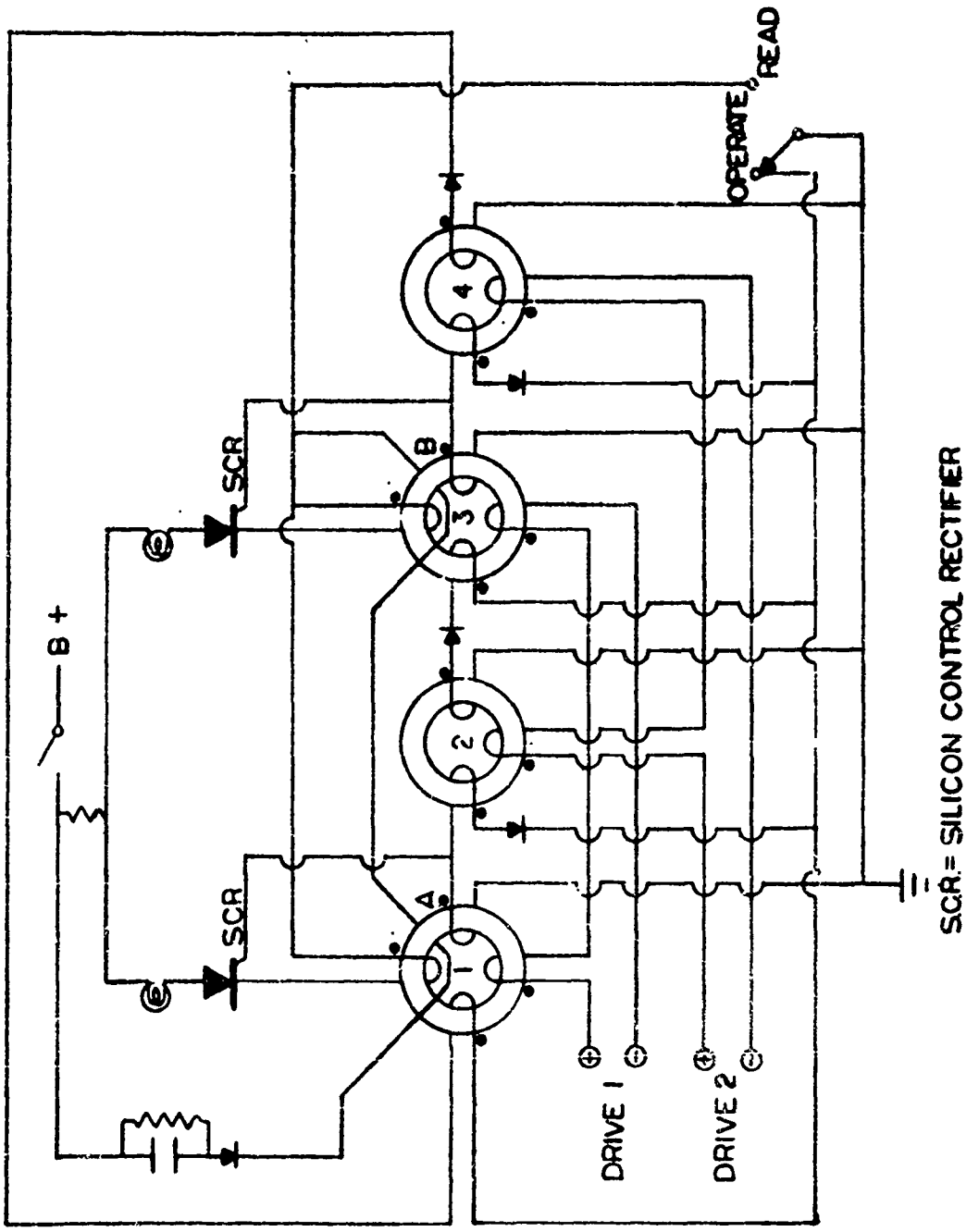


Figure 17. Readout circuit

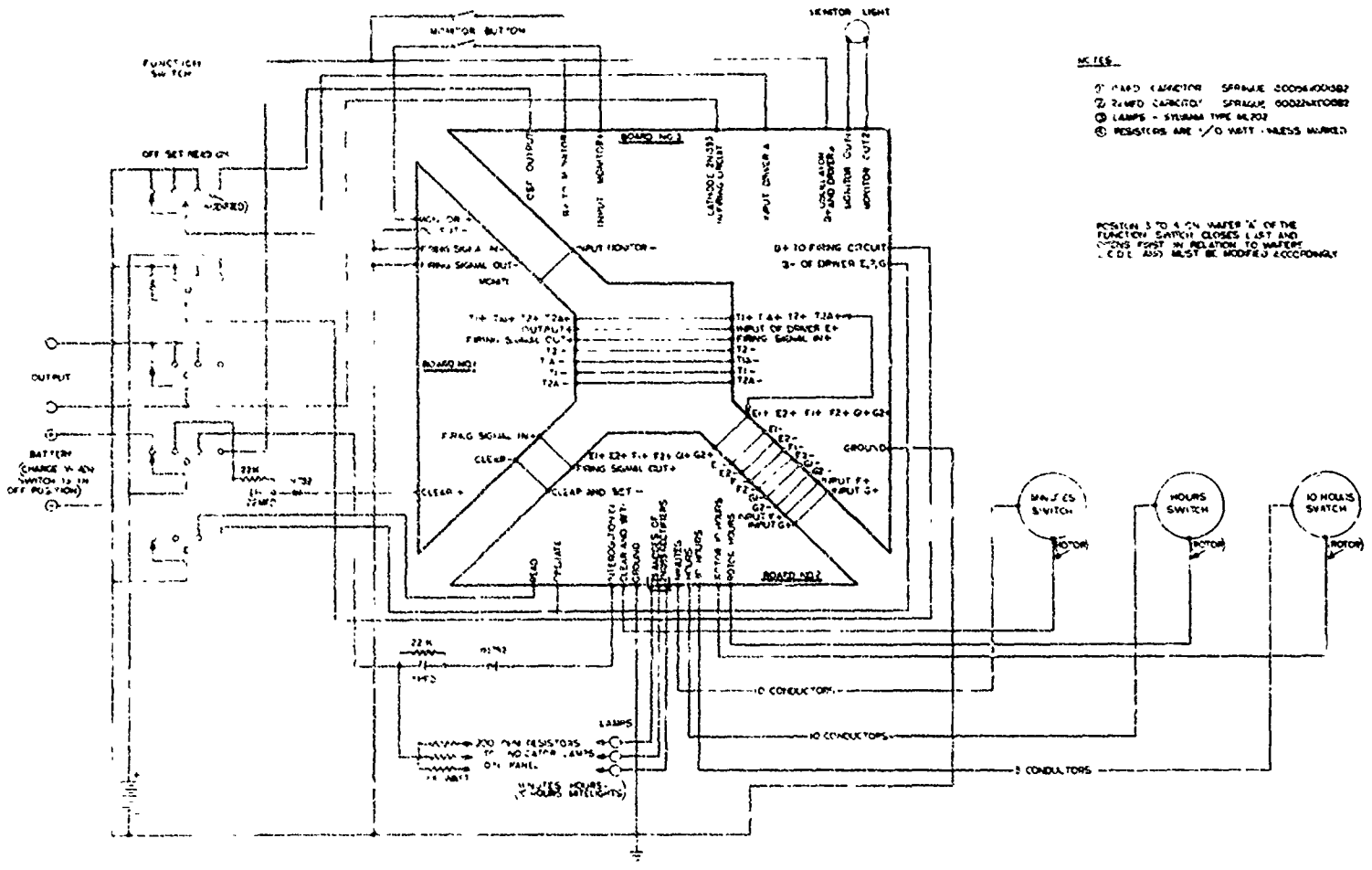
11. POWER SUPPLY

The power supply chosen was a six-cell silver oxide-zinc type battery. The cells are manufactured by the Eagle-Picher Corporation No. 2495 low-rate series A cells. They have a nominal voltage of 1.55 v. They may be recharged about five times. To recharge, the cells are discharged down to a cell voltage of 1.20 v and then charged at 0.5 amp until the cell voltage is raised to 2.0 v. Under no circumstances should the charging voltage be allowed to exceed 2.1 v. At a 20-ma drain, the current drawn by the entire timer, the cells have a room temperature life of 100 hr. Below -30C the life of the cells drops off drastically both in ampere-hour capacity and and in cell voltage. At the present time this type of cell has the highest energy per unit volume of any cell commercially available. The power supply still remains a problem. No intensive effort was made to investigate batteries under the interpretation of the scope of work. An independent effort is to be made. However, from the outset it was realized that the power supply would be a problem and every effort was made to alleviate the difficulty by using low-energy circuits. All temperature tests of the timers were made with the power supply external to the temperature chamber. It should be noted that DOFL has made significant advances with this type of cell and the expectation is that performance will be extended down to -55C.

12. FUNCTION SWITCH

The function switch is a nonshorting, two-deck switch. Each deck has three poles and four positions. Five of the six poles are used (fig. 18). The four positions are OFF, SET, READ, and ON. The switch performs the following functions:

	Position			
Pole	OFF	SET	READ	ON
A	Oscillator output grounded	Oscillator output grounded	Oscillator output grounded	Oscillator connected to driver
B	Firing circuit B+ lead grounded	Firing circuit B+ lead grounded	Firing circuit B+ lead grounded	B+ to firing circuit
C	OUTPUT terminals shorted	OUTPUT terminals shorted	OUTPUT terminals shorted	OUTPUT terminals in firing circuit
D	Battery may be charged at BATTERY terminals	B+ to SET	B+ to interrogate and readout lamps	B+ to monitor, oscillator, and drivers
E	Settable shift register loops open, readout ground open	Loops open, readout ground open	Loops open, readout ground closed	Loops closed, readout ground open



NOTES

1. 1 MFD CAPACITOR SPRAGUE 30D106X0035B2
2. 2 MFD CAPACITOR SPRAGUE 30D226X0035B2
3. LAMPS - SYLVANIA TYPE #1202
4. RESISTORS ARE 1/2 WATT UNLESS MARKED

POSITION 3 TO 4 ON WAFER "A" OF THE FUNCTION SWITCH CLOSES LAST AND OPENS FIRST IN RELATION TO WAFERS 1,2,B,C AND MUST BE MODIFIED ACCORDINGLY

Figure 18. Function switch and printed circuit board interconnections 1707-61

Pole A is modified so that when going between READ to ON, it closes last and opens first in relation to poles B, C, D, and E. The purpose of this is to retain the bits in the timer. For example, if the loops were open and the oscillator pulsed the drivers, the bits would be lost. Bits could also be lost if the oscillator pulsed the driver before the 22-μf capacitor in the driver charged up. With the oscillator connected last and broken first, these modes of losing bits are eliminated. It should be noted that the first pulse out of the oscillator takes place about 0.01 sec after the applications of B+ to the oscillator.

13. EVALUATION

The circuits used in the timer were temperature tested individually and when assembled together. Individually all circuits worked over the temperature range except the readout circuit. The readout circuit did not work below 0C . The reason was traced to the sensitivity of the 2N1595 SCR. Examination showed that the majority of these units did not meet the manufacturer's specifications for sensitivity. Further inquiry disclosed that Solid State Products could supply an SCR in one-fifth the volume of the 2N1595. Specifications of the SCR for the readout circuit were set up with Solid State Products and the samples supplied easily met the requirements for the readout circuit. The SCR's (No. 3D1017) having the desired specifications can be purchased from Solid State Products. Because of lack of time, these SCR's were not used in the prototypes.

After assembly and at about -20C the monitor circuit would not blink, although the timer continued to count. This was traced to the input signal to the monitor. As the temperature dropped, the gain of the 2N704 transistors dropped slightly and the monitor circuit became less sensitive. The input signal was low by about 0.5 v to trigger it. The input diode was replaced by a 0.1-μf capacitor in the breadboard and the unit worked. A better solution is thought to be either to increase the bias on the input 2N703, or to use a separate winding with more turns on core AN1, or to use the pulse when the "one" is going into the AN1 rather than when it is being transferred out. Possibly a combination of the above would be the most reliable solution. Since the replacement of the diode with a capacitor was not thought to give enough margin for reliable operation and since the other schemes were not completely investigated, the prototypes were left with the diodes intact.

The temperature range over which the unit was tested was -55C to +75C. The power supply was varied from 8.4 to 10.8 v for all temperature tests.

14. CONCLUSIONS AND RECOMMENDATIONS

This study has shown that it is feasible to meet the specifications for the timer and that the task is well within the state of the electronic art. The following recommendations are made if further investigation is to follow.

(a) Consider the use of the miniature tuning fork oscillator similar to the one manufactured by the Bulova Watch Company. Temperature cycling of the oscillator has shown its accuracy to be more than ±0.1 percent. Its power consumption is extremely low and could cut the total current requirement of the timer from 20 ma to about 5 ma.

(b) Add Zener diode control to the drivers as described in section 3. This would allow the timer to work over a greater voltage variation and relax the battery requirement.

(c) Replace the transistors in the driver with smaller transistors of equal or better characteristics.

(d) Examine the use of voltage drive for the shift registers.

(e) Design a coincident current and a transistor AND circuit and evaluate them in comparison with the present AND circuit.

(f) Incorporate the design changes for the monitor outlined in section 6.

(g) Use the 3D1017 SCR in the readout circuit.

(h) Eliminate the separate set winding and use the three-turn loop winding for this function.

(i) Assemble the magnetic cores on their sides instead of on their ends and use 100 percent printed circuitry for the shift registers. Small pilot shift registers have been made using this technique and this type of register has proved highly advantageous over the original packaging technique.

(j) The set switches and the readout lamps should be integral with the printed circuit board containing the three settable shift registers. This is to minimize the number of interconnections between assemblies.

APPENDIX A

UNIJUNCTION TRANSISTOR OSCILLATOR

1. PERFORMANCE CHARACTERISTICS

Table A1. Unijunction Transistor Oscillator Performance Characteristics [a]

Temperature (^{o}C)	Oscillator No. 1 (sec) [b]	Oscillator No. 2 (sec) [b]
+75	.010010	.010010
+65	.010013	.010013
+55	.010011	.010011
+45	.010005	.010011
+35	.009998	.010006
+25	.009989	.010003
+15	.009977	.009991
+ 5	.009968	.009984
- 5	.009965	.009974
-15	.009970	.009972
-25	.009983	.009971
-35	.009997	.009978
-45	.009994	.009998
-55	.0099620	.010017

[a] See figure A1.

[b] Target period 0.009990 sec

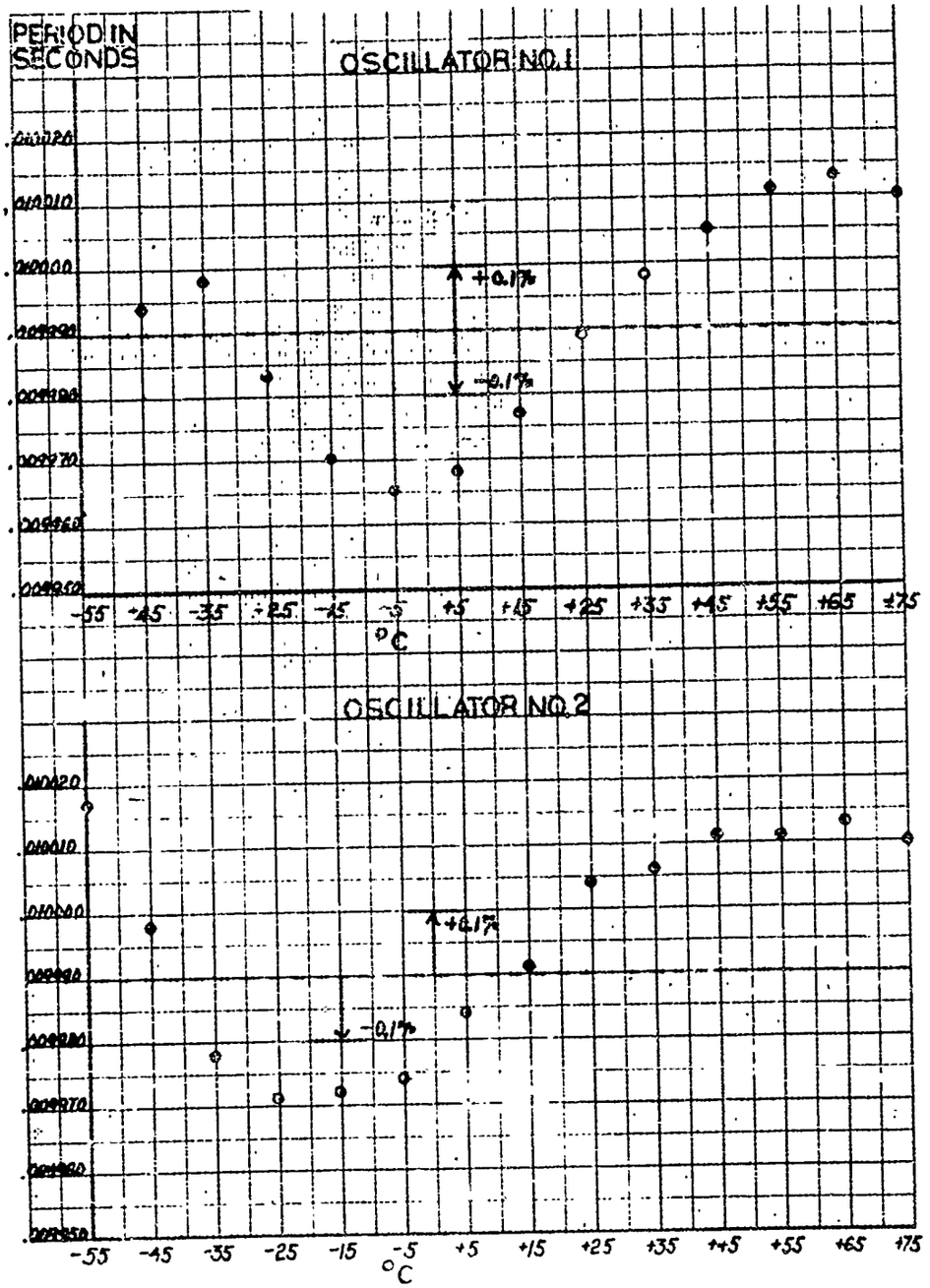


Figure A1. Unijunction transistor oscillator temperature performance.

2. OPERATING INSTRUCTIONS

(a) With the function switch in the OFF position, set the desired function time.

(b) Turn the function switch to SET and then to READ.

(c) Verify the set in function time against the read time.

(d) Turn the function switch to ON.

(e) Check timer operation by pressing the monitor button. If the timer is counting, the monitor light should blink on and off continuously as long as the monitor button is pressed.

(f) The time remaining to fire may be read out by moving the function switch to READ. Timer operation is resumed when the function switch is turned to ON.

(g) To reset, turn function switch to OFF and repeat steps (1) through (6).

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TR-995, 12 December 1961, 19 pp text, 19 illus, DA5N12-15-030, OMS 5530.12.58900.03, DOFL Proj 45400 - UNCLASSIFIED REPORT

A settable all-electronic long-delay timer is described. The timer is settable in five-minute increments from five minutes to forty-nine hours fifty-five minutes. At the end of the set-in time a silicon controlled rectifier is latched on that is capable of delivering 2 amp at 6 v. The time remaining to fire may be read out upon command at any time. The time base is a 100.1 cps unijunction transistor oscillator. Countdown is by magnetic core shift registers. The total volume for the timer and its 100-hr power supply is 35 in^3.

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AD________ Accession No.__________ Timer, electronic — Long-delay

Diamond Ordnance Fuze Laboratories, Washington 25, D. C.

ELECTRONIC LONG-DELAY TIMER - Ira Marcus

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REMOVAL OF EACH CARD WILL BE NOTED ON INSIDE BACK COVER, AND REMOVED CARDS WILL BE TREATED AS REQUIRED BY THEIR SECURITY CLASSIFICATION.